ABSTRACT

A nonvolatile semiconductor storage unit can prevent erratic sense operations in a sense latch circuit by adopting a single-end sensing system capable of reducing an area (decreasing the number of elements). There is provided a flash memory chip using the single-end sensing system and an NMOS gate sensing system together. In the single-end sensing system, the sense latch circuit is connected to one end of a global bit line to detect data on the global bit line corresponding to a threshold voltage for a memory cell. The NMOS gate sensing system uses an NMOSFET to receive data on the global bit line at a gate and drive a node for the sense latch circuit. The NMOSFET senses a sense voltage. The sense latch circuit is activated with a sufficient signal quantity ensured. An output voltage from a threshold voltage applying power supply precharges the global bit line. In this manner, it is possible to always keep a constant difference between a precharge voltage and a threshold voltage for the NMOSFET.